### 2097152-BIT(262144-WORD BY 8-BIT)CMOS STATIC RAM

#### **DESCRIPTION**

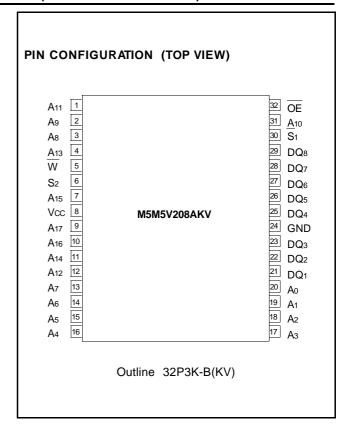
The M5M5V208AKV is low voltage 2-Mbit static RAMs organized as 262,144-words by 8-bit, fabricated by high-performance  $0.25\mu m$  CMOS technology.

The M5M5V208AKV is suitable for memory applications where a simple interfacing , battery operating and battery backup are the important design objectives.

The M5M5V208AKV is packaged in 32-pin 8mm x 13.4mm sTSOP packages which is a high reliability and high density surface mount device.

### **FEATURES**

	Access	Power supply cur			
Type name			stand-by (max)		
M5M5V208AKV-55HI	55ns	35mA (10MHz)	30µA (Vcc=3.6V)		
M5M5V208AKV-70HI	70ns	7mA (1MHz)	0.3µA (Vcc=3.0V TYPICAL)		



- Single 2.7 ~3.6V power supply
- No clock, No refresh
- Directly TTL compatible : All inputs and outputs
- Easy memory expansion and power down by  $\overline{\text{S1}}, \text{S2}$
- Data hold on +2V power supply
- Three-state outputs : OR tie capability
- OE prevents data contention in the I/O bus
- Common data I/O
- Package

M5M5V208AKV ...... 32pin 8 X 13.4 mm sTSOP

### **FUNCTION**

The operation mode of the M5M5V208AKV series are determined by a combination of the device control inputs  $\overline{S}_1,S_2,\overline{W}$  and  $\overline{OE}$ .

Each mode is summarized in the function table.

A write cycle is executed whenever the low level W overlaps with the low level S1 and the high level S2. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of  $\overline{W}$ ,  $\overline{S1}$  or S2, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input  $\overline{OE}$  directly controls the output stage. Setting the  $\overline{OE}$  at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting  $\overline{W}$  at a high level and  $\overline{OE}$  at a low level while  $\overline{S_1}$  and  $S_2$  are in an active state( $\overline{S_1}$ =L, $S_2$ =H).

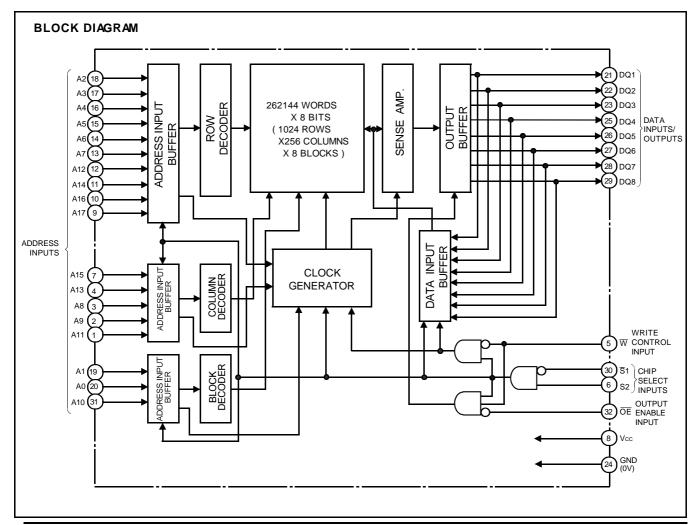
When setting  $\overline{S_1}$  at a high level or  $S_2$  at a low level, the chip are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high- impedance state, allowing ORtie with other chips and memory expansion by  $\overline{S_1}$  and  $S_2$ . The power supply current is reduced as low as the stand-by current which is specified as Icc3 or Icc4, and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

### **FUNCTION TABLE**

S <sub>1</sub>	S <sub>2</sub>	W	OE	Mode	DQ	Icc
Χ	L	Χ	Χ	Non selection	High-impedance	Stand-by
Н	Χ	Χ	Χ	Non selection	High-impedance	Stand-by
L	Н	L	Х	Write	Din	Active
L	Н	Н	L	Read	Dout	Active
L	Н	Н	Н		High-impedance	Active

Note 1: "H" and "L" in this table mean VIH and VIL, respectively.

<sup>2: &</sup>quot;X" in this table should be "H" or "L".



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### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		- 0.5*~4.6	V
Vı	Input voltage	With respect to GND	- 0.5*~Vcc + 0.3	V
Vo	Output voltage	What respect to GIVE	0~Vcc	V
Pd	Power dissipation	Ta=25°C	700	mW
Topr	Operating temperature		- 40~85	°C
Tstg	Storage temperature		- 65~150	°C

<sup>\* -3.0</sup>V in case of AC ( Pulse width ≤ 30ns )

# DC ELECTRICAL CHARACTERISTICS (Ta= -40~85°C, Vcc=2.7~3.6V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
Symbol	Farameter	rest conditions		Min	Тур	Max	Offic
VIH	High-level input voltage			2.0		Vcc + 0.3	V
VIL	Low-level input voltage			-0.3*		0.6	V
Voh1	High-level output voltage 1	Iон= - 0.5mA		2.4			V
VOH2	High-level output voltage 2	Iон= - 0.05mA					V
Vol	Low-level output voltage	IoL=2mA	IoL=2mA			0.4	V
lı	Input current	Vi=0~Vcc				±1	μΑ
lo	Output current in off-state	S1=VIH or S2=VIL or OE=VIH VI/0=0~Vcc				±1	μΑ
Active supply current	Active supply current $\frac{-}{S_1} \le 0.2V, S_2 \ge Vcc-0.2V$	10MHz		28	30		
ICC1	, touve supply surroun	OS-level input) other inputs ≤ 0.2V or ≥ Vcc-0.2V, Output-open	1MHz		5	7	mA
	Active supply current	S1=VIL,S2=VIH,	10MHz		33	35	
ICC2	(TTL-level input)	other inputs=VIH or VIL, Output-open	1MHz		5	7	mA
			~25°C		0.3	2	
loos	0. 11	1) S₂ ≤ 0.2V, other inputs=0 ~ Vcc	~40°C			5	
ICC3	Stand-by current	2) S1 ≥ Vcc - 0.2V, S2 ≥ Vcc - 0.2V other inputs=0 ~ Vcc	~70°C			10	μA
		~{				30	
ICC4	Stand-by current	1) \$\overline{S}_1=VIH\$, other inputs=VIL or VIH 2) \$S_2=VIL\$, other inputs=VIL or VIH				0.33	mA

 $<sup>^{\</sup>ast}$  -3.0V in case of AC ( Pulse widths 30ns )

### CAPACITANCE (Ta=- 40~85°C, unless otherwise noted)

	Demonstra					
Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
Сі	Input capacitance	Vi=GND, Vi=25mVrms, f=1MHz			8	pF
Co	Output capacitance	Vo=GND.Vo=25mVrms. f=1MHz			10	pF

Note 3: Direction for current flowing into an IC is positive (no mark).



<sup>4:</sup> Typical value is Vcc = 3V, Ta = 25°C

### AC ELECTRICAL CHARACTERISTICS (Ta=- $40 \sim 85$ °C, unless otherwise noted )

# (1) MEASUREMENT CONDITIONS

Vcc ----- 2.7~3.6V

Input pulse level ..... VIH=2.2V, VIL=0.4V

Input rise and fall time... 5ns

CL=5pF (for ten,tdis)

Transition is measured ± 500mV from steady

state voltage. (for ten,tdis)

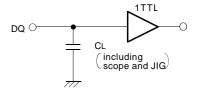


Fig.1 Output load

### (2) READ CYCLE

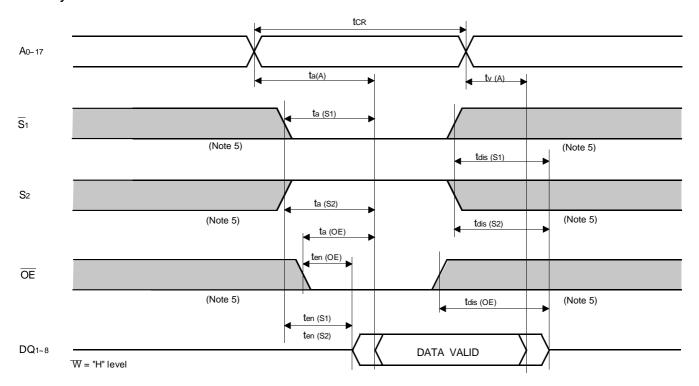
		Limits		Limits			
Symbol	Parameter	-55	HI	-70	HI	Unit	
		Min	Max	Min	Max	0111	
tcr	Read cycle time	55		70		ns	
ta(A)	Address access time		55		70	ns	
ta(S1)	Chip select 1 access time		55		70	ns	
ta(S2)	Chip select 2 access time		55		70	ns	
ta(OE)	Output enable access time		30		35	ns	
tdis(S1)	Output disable time after \$\overline{S}_1\$ high		20		25	ns	
tdis(S2)	Output disable time after S2 low		20		25	ns	
tdis(OE)	Output disable time after OE high		20		25	ns	
ten(S1)	Output enable time after \$\overline{S_1}\$ low	10		10		ns	
ten(S2)	Output enable time after S <sub>2</sub> high	10		10		ns	
ten(OE)	Output enable time after OE low	5		5		ns	
tV(A)	Data valid time after address	10		10		ns	

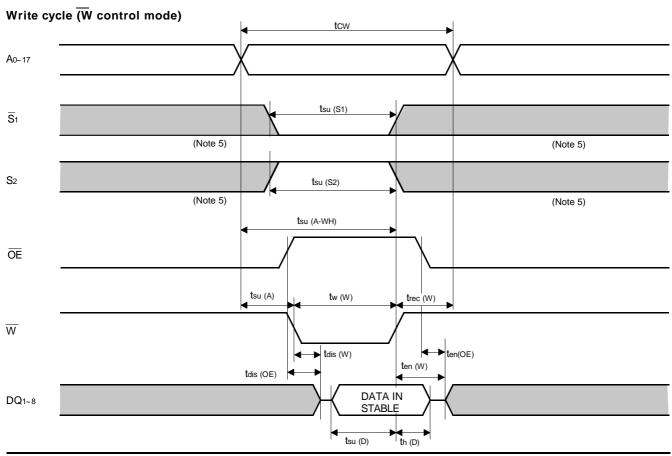
### (3) WRITE CYCLE

			Lim	Limits		
Symbol	Parameter	-5	5HI	-70	IHC	Unit
		Min		Min	Max	
tcw	Write cycle time	55		70		ns
tw(W)	Write pulse width	45		55		ns
tsu(A)	Address setup time	0		0		ns
tsu(A-WH)	Address setup time with respect to $\overline{W}$	50		65		ns
tsu(S1)	Chip select 1 setup time	50		65		ns
tsu(S2)	Chip select 2 setup time	50		65		ns
tsu(D)	Data setup time	25		30		ns
th(D)	Data hold time	0		0		ns
trec(W)	Write recovery time	0		0		ns
tdis(W)	Output disable time from W low		20		25	ns
tdis(OE)	Output disable time from OE high		20		25	ns
ten(W)	Output enable time from W high	5		5		ns
ten(OE)	Output enable time from OE low	5		5		ns

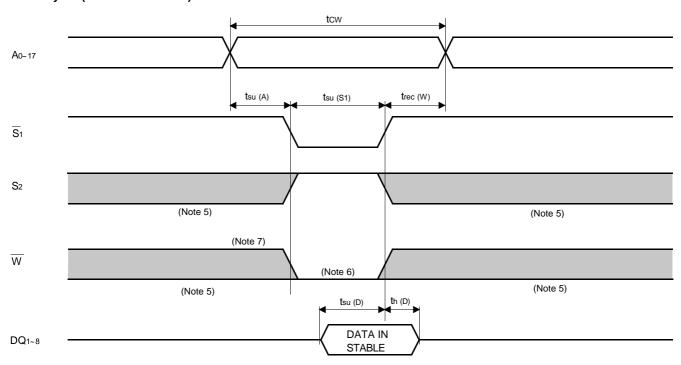


# (4) TIMING DIAGRAMS Read cycle

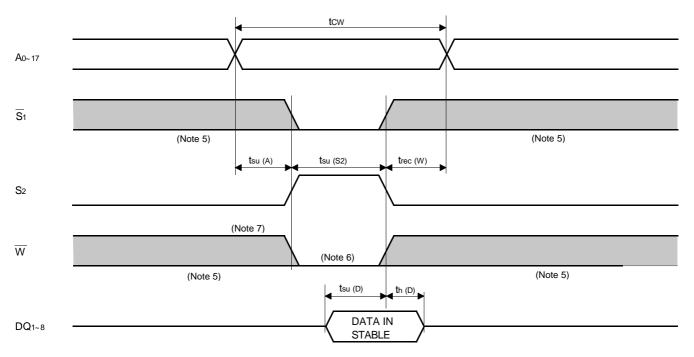




# Write cycle (S1 control mode)



### Write cycle (S2 control mode)



 $\begin{array}{ll} \text{Note} & \text{5: Hatching indicates the state is "don't care".} \\ & \text{6: Writing is executed while $S_2$ high overlaps $\overline{S_1}$ and $\overline{W}$ low.} \end{array}$ 

7: When the falling edge of  $\overline{W}$  is simultaneously or prior to the falling edge of  $\overline{S}_1$  or rising edge of  $S_2$ , the outputs are maintained in the high impedance state.

8: Don't apply inverted phase signal externally when DQ pin is output mode.



### POWER DOWN CHARACTERISTICS

### (1) ELECTRICAL CHARACTERISTICS (Ta= -40~85°C, unless otherwise noted)

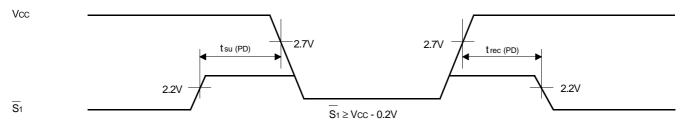
0	5 .		Limits				
Symbol	Parameter	Test conditions	l est conditions		Тур	Max	Unit
VCC (PD)	Power down supply voltage			2.0			V
VI (S1)	Chip select input \$\overline{S}_1\$			2.0			V
VI (S2)	Chip select input S2					0.2	V
		Vcc = 3.0V	~25°C		0.3	1	
		1) S₂ ≤ 0.2V, other inputs = 0~Vcc	~40°C			3	
ICC (PD)	Power down supply current	2) \$\overline{S_1}\$ ≥ Vcc-0.2V, \$2 ≥ Vcc-0.2V, other inputs = 0~Vcc	~70°C			8	μA
		otrier riputs – 0~ vcc	~85°C			24	

### (2) TIMING REQUIREMENTS (Ta=-40~85°C, unless otherwise noted )

Symbol	Parameter	Test conditions	Min	Тур	Max	Unit
tsu (PD)	Power down set up time		0			ns
trec (PD)	Power down recovery time		5			ms

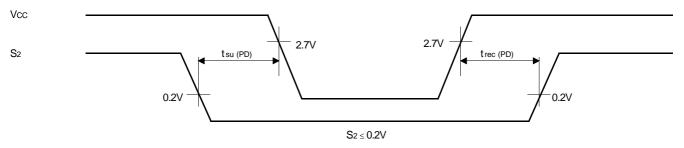
### (3) POWER DOWN CHARACTERISTICS

# S<sub>1</sub> control mode



Note 9: On the power down mode by controlling  $\overline{S_1}$ , the input level of  $S_2$  must be  $S_2 \ge Vcc$  - 0.2V or  $S_2 \le 0.2V$ . The other pins(Address,I/O,WE,OE) can be in high impedance state.

### S<sub>2</sub> control mode



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